

**IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
TYLER DIVISION**

UNILOC USA, INC. and UNILOC
LUXEMBOURG S.A.,

Plaintiffs,

v.

RACKSPACE HOSTING, INC. and
RACKSPACE US, INC.,

Defendants.

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CIVIL ACTION NO. 6:12-cv-00375

JURY TRIAL DEMANDED

**PLAINTIFFS' OPPOSITION TO DEFENDANTS' DISMISS FOR FAILURE
TO ALLEGE INFRINGEMENT OF A PATENABLE CLAIM UNDER 35 U.S.C. § 101**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	SUMMARY OF ARGUMENTS IN FAVOR OF CLAIM 1	3
III.	BACKGROUND OF THE '697 PATENT.....	3
IV.	THE INVENTION DESCRIBED IN CLAIM 1	4
V.	ARGUMENTS AND AUTHORITIES.....	6
	A. Claim 1 Does Not Describe a Mathematical Algorithm	7
	B. Claim 1 is Not an Abstract Expression	9
	C. Machine or Transformation Test is Not Dispositive.....	11
VI.	CLAIMS 2 - 28	12
VII.	CONCLUSION.....	14

TABLE OF AUTHORITIES

CASES

Bilski v. Kappos,
130 S. Ct. 3218 (2010).....7, 11

Diamond v. Diehr,
450 U.S. 175 (1981).....7

Doe ex rel. Doe v. Dallas Indep. Sch. Dist.,
153 F.3d 211 (5th Cir. 1998)2

Gottschalk v. Benson,
409 U.S. 63 (1972).....7, 8, 9

In re Bilski,
545 F.3d 943, 951 (Fed. Cir. 2008).....2

Lormand v. US Unwired, Inc.,
565 F.3d 228, 232 (5th Cir. 1998)1

Mackay Radio & Tel. Co. v. Radio Corp. of America,
306 U.S. 86, 94 (1939).....9

Matsushita Elec. Indus. Co. v. Zenith Radio Corp.,
475 U.S. 574, 587 (1986).....1

Microsoft Corp. v. i4i Ltd. P’ship,
131 S. Ct. 2238, 2242 (2011).....1

Parker v. Flook,
437 U.S. 584, 588 (1978).....8, 9

Prompt Med. Sys., L.P. v. AllscriptsMysis Healthcare Solutions, Inc.,
No. 6:10-CV-71, 2012 U.S. Dist. LEXIS 30694 (E.D. Tex. Feb. 13, 2012).....11

Research Corp. Techs. v. Microsoft Corp.,
627 F.3d 859, 868 (Fed. Cir. 2010).....9, 10, 11

State St. Bank & Trust Co. v. Signature Fin. Group,
149 F.3d 1368, 1370 (Fed. Cir. 1998).....2

Ultramercial, LLC v. Hulu, LLC,
657 F.3d 1323, 1327 (Fed. Cir. 2011).....11

STATUTES & AUTHORITIES

Rule 12(b)(6)..... 1-2, 14

35 U.S.C. § 101.....1-3, 6-8, 11-14

35 U.S.C. § 112.....12

35 U.S.C. § 282.....1

Plaintiffs, Uniloc USA, Inc. and Uniloc Luxembourg S.A. (together “Uniloc”), respectfully submit this opposition to Defendants’ Motion to Dismiss Uniloc’s Complaint for Failure to Allege Infringement of a Patentable Claim under 35 U.S.C. § 101. For the reasons set forth herein, Defendants’ motion should be denied.

Uniloc alleges that Defendants Rackspace Hosting, Inc. and Rackspace US, Inc. (collectively, “Rackspace”) have infringed and continue to infringe United States Patent No. 5,892,697 (the “‘697 patent”). In lieu of answering, Rackspace filed a motion to transfer the case to the Western District of Texas (Dkt. No. 17) and the present motion to dismiss under Rule 12(b)(6).

I. INTRODUCTION

In the Fifth Circuit, a Rule 12(b)(6) motion to dismiss for failure to state a claim “is viewed with disfavor and rarely granted.” *Lormand v. US Unwired, Inc.*, 565 F.3d 228, 232 (5th Cir. 2009). Rackspace’s Motion, however, does not argue that Uniloc’s Complaint suffers from a pleading defect; rather, it seeks summary judgment of invalidity. By using Rule 12(b)(6) to cloak what is otherwise a request for judgment on the merits, Rackspace seeks to circumvent the rigorous clear and convincing evidence standard required to invalidate a patent presumed valid by statute. 35 U.S.C. § 282; *see also Microsoft Corp. v. i4i Ltd. P’ship*, 131 S. Ct. 2238, 2242 (2011) (“We consider whether § 282 requires an invalidity defense to be proved by clear and convincing evidence. We hold that it does.”); *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 587 (1986) (“[on] summary judgment the inferences to be drawn from the underlying facts . . . must be viewed in the light most favorable to the party opposing the motion.”).

Because of this, Rackspace's Motion is untimely and not the appropriate vehicle to raise arguments related to the validity of the asserted patent under 35 U.S.C. § 101, especially given that infringement contentions have not been served nor has there be a claim construction ruling in this case. *See Doe ex rel. Doe v. Dallas Indep. Sch. Dist.*, 153 F.3d 211, 220 (5th Cir. 1998) ("The Rule 12(b)(6) motion . . . must be distinguished from a motion for summary judgment under Rule 56, which goes to the merits of the claim and is designed to test whether there is a genuine issue of material fact. The Rule 12(b)(6) motion...only tests whether the claim has been adequately stated in the complaint."); *see also In re Bilski*, 545 F.3d 943, 951 (Fed. Cir. 2008) (In analyzing validity under 35 U.S.C. § 101, claim construction "is an important first step.") (citing *State St. Bank & Trust Co. v. Signature Fin. Group*, 149 F.3d 1368, 1370 (Fed. Cir. 1998) (noting that whether a claim is invalid under § 101 "is a matter of both claim construction and statutory construction")). Accordingly, the Motion should be dismissed on these grounds alone.

Despite the foregoing, Uniloc generally agrees with Rackspace that a quick resolution of this issue on the merits will advance this litigation. Therefore, Uniloc will dedicate most of this Opposition to addressing the merits of Rackspace's arguments concerning whether the claims of United States Patent No. 5,892,697 (the "'697 Patent") meet the requirements for patentability under 35 U.S.C. § 101.

In addition, to further narrow the issues, Uniloc represents to the Court that it will only be asserting Claim 1 of the '697 Patent against Rackspace in this lawsuit. While Uniloc is not required to make this decision at this time (as no date for the serving of infringement contentions has been set), Uniloc believes such election will allow the Court to most efficiently focus on the one claim at issue in this suit instead of the 27 other claims of the '697 Patent. Accordingly, Uniloc's arguments, found below, primarily involve Claim 1 of the '697 Patent.

II. SUMMARY OF ARGUMENTS IN FAVOR OF CLAIM 1

This Court should deny Rackspace's request to dismiss Uniloc's claims of infringement, as the claims of the asserted patent meet the requirements for patentability under 35 U.S.C § 101. Rackspace's motion, which relies heavily on the Supreme Court's *Benson* decision, is based on a mischaracterization of the inventions described in the '697 Patent. As will be shown below, the '697 Patent describes and claims an improved way to process certain types of numbers inside a computer. This process is neither a mathematical formula nor an abstract idea and therefore falls within the zone of subject matter eligible for patent protection under 35 U.S.C § 101.

III. BACKGROUND OF THE '697 PATENT

The '697 Patent describes an improved method and apparatus to process floating-point numbers. '697 Patent (Dkt. No. 1-2), Col. 1:8-9. Floating-point numbers are numbers having digits to the right of the decimal point in a computer (*e.g.*, 12.897). Floating-point numbers described in the '697 Patent have at least three fields: (i) a sign (to indicate whether the number is positive or negative), (ii) an exponent field (which allows for the representation of very large or small numbers) and (iii) a mantissa (the "body" of the number). '697 Patent, Col. 1:18-32. Due to their nature, digital computers (both at the time of the invention and today) have to process floating-point numbers in a significantly different way than integers. Thus, adding 2 and 2 together is, from a computer's standpoint, very different than adding 2.1 and 2.1.

Not only is the computation of floating-point numbers different, it is more difficult than processing integers. The adding of 2 and 2 is a trivial operation for a computer, compared to adding 2.1 and 2.1. This complexity stems, in part, from having to process the various fields that make up the floating-point number. In many instances, microprocessors have dedicated circuits

to process floating-point numbers. '697 Patent, Col. 2:36-46.

When a particular floating point number is not being operated on, it may be stored in memory (*i.e.*, RAM) associated with the microprocessor. But, when the floating-point number is to be operated on by the microprocessor, it is moved into a special memory unit called a register. Once in the correct register, the microprocessor can perform arithmetic computations on the number. *Id.*

In the early 1980's, the Institute of Electrical and Electronics Engineers (IEEE) standardized a method for processing floating-point numbers in a computer. See '697 Patent, Col. 1:18-21. This standard was promulgated as IEEE Standard 754. This Standard ultimately enjoyed wide adoption, and was implemented in various Intel processors that powered billions of PCs around the world. *See* Exh. A, p. 6 ("According to one IEEE 754 revision committee member, [the Standard] has been the 'pivotal flagship example of IEEE standards and one of the most implemented and far-reaching of any IEEE standard.' Since 1984, more than 1.2 billion Intel processors alone have confirmed to the [IEEE 754 Standard]."). While this standard was helpful in presenting a unified process by which computer manufacturers and software developers could perform arithmetic computations on floating point numbers, it was computationally time intensive to implement certain portions of the standard. '697 Patent, Col. 2:24-35. Thus, efforts were made to improve the standard to cut down on the time it took to process floating point numbers.

IV. THE INVENTION DESCRIBED IN CLAIM 1

As described in the '697 Patent, Claim 1 outlines improvements to the IEEE Standard and the processing of floating-point numbers in general. First, the inventor of the '697 Patent realized that the format of a floating-point number, as stored in memory (*i.e.*, RAM), may not be

the optimal format for the number once it is loaded into a register. '697 Patent, Col. 2:36-46. Given that millions (or perhaps billions) of floating-point numbers can be stored in RAM associated with a microprocessor, it is important to minimize the amount of memory used to store each number. But, when a floating-point number is moved to a register, of which there are relatively few, the format of the number needs to be optimized for speed of processing (*i.e.*, the amount of memory used to store the number in a register is not as important a consideration as when the number is stored in memory). *Id.*

Second, the inventor also realized that computational efficiencies could be realized over what was present in the IEEE Standard if the operand (*i.e.*, the number on which a computation is to be performed) is rounded *prior* to the actual arithmetic operation, as opposed to rounding the result of the operation itself. As stated in the '697 Patent:

Utilizing the value in the floating-point register converted by the load means from the memory register, the arithmetic logic means performs its computation upon the operand. However, prior to doing so it first rounds the value. By rounding, the arithmetic logic means replaces the inaccurate portion of the mantissas of the arithmetic unit operands by either all zero bits, all one bits, the accuracy section of the mantissa, or the complement of the accuracy section. Rounding, and thereby adjusting, the operand is contrary to the IEEE 754 rounding of results. The benefit of rounding the operand instead of the result is that carry propagation is eliminated and no exponent adjustment is required. Additionally, due to the lack of result rounding, arithmetic operations have a more efficient implementation. In particular, it becomes possible to have fewer pipeline stages or eliminate conditionally performed pipeline stages thereby shortening the total logic delay of the arithmetic operation.

'697 Patent, Col. 4:32-48 (emphasis added). In other words, '697 Patent goes against the teaching of the IEEE 754 standard by rounding a number before a mathematical operation is performed on the number, thereby allowing for a more efficient processing of the number.

These advancements are captured in the language of Claim 1, presented below. The middle column recites the actual claim language, while the right hand column describes how the

corresponding step achieves the benefits of the invention.

<u>Step No.</u>	<u>Claim Element</u>	<u>Description of the Step</u>
	A method for processing floating-point numbers, each floating-point number having at least a sign portion, an exponent portion and a mantissa portion, comprising the steps of:	The preamble sets forth the components of the floating point number to be processed.
1	converting a floating-point number memory register representation to a floating-point register representation;	The format of the floating-point number is changed from how it is represented in memory to how it is represented in a floating-point register.
2	rounding the converted floating-point number;	The floating-point number is rounded <i>prior</i> to being operated upon.
3	performing an arithmetic computation upon said rounded number resulting in a new floating-point value;	An arithmetic computation is performed on the rounded floating-point number.
4	converting the resulting new floating-point register value to a floating-point memory register representation.	Finally, the format of the new floating-point number is converted back to the format used to store the number in memory.

V. ARGUMENTS AND AUTHORITIES

Title 35 U.S.C. § 101 states that “[w]hoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.”

Claim 1, which by its own terms and read in the context of the ‘697 Patent, describes an improved method for processing floating-point numbers. The Claim itself then lists a number of process steps by which floating-point numbers are processed. In the absence of any other authority, this explanation alone should settle any issues about the patentability of Claim 1 under 35 U.S.C. § 101 - the Claim purports to be an improvement of an existing process by which

floating-point numbers are processed - which is statutory subject matter by the very words of the statute.

But, as most recently stated by the Supreme Court, there are “three specific exceptions to § 101’s broad patent-eligibility principles: ‘laws of nature, physical phenomena, and abstract ideas.’ While these exceptions are not required by the statutory text, they are consistent with the notion that a patentable process must be ‘new and useful.’” *Bilski v. Kappos*, 130 S. Ct. 3218, 3225 (2010) (internal citations omitted). Rackspace states that Claim 1 falls into two of these exceptions: (1) the Claim is unpatentable because it is a mathematical formula/algorithm (and hence a “law of nature’), *see Diamond v. Diehr*, 450 U.S. 175, 186 (1981) (“We defined ‘algorithm’ as a ‘procedure for solving a given type of mathematical problem,’ and we concluded that such an algorithm, or mathematical formula, is like a law of nature, which cannot be the subject of a patent.”), and (2) the Claim is unpatentable because it is an abstract idea. These are distinct concepts and will be addressed separately below.

A. Claim 1 Does not Describe a Mathematical Algorithm

Rackspace repeatedly states that Claim 1 recites a mathematical formula or an unpatentable algorithm. This is incorrect, as Claim 1 does not recite any general mathematical algorithm, let alone a particular mathematical formula of the type found improper in *Benson*. *See generally Gottschalk v. Benson*, 409 U.S. 63 (1972). Instead, Claim 1 covers a method for generally processing floating-point numbers. Such a determination can be made from a simple inspection of the “performing” step in Claim 1 (step 3). This step requires an arithmetic computation to be performed, but is not limited to any particular one. It could be multiplication, division, a logarithmic operation, etc. Likewise, the conversion steps do not require the application of any particular mathematical formula, let alone recite a mathematical formula.

The lack of a specific mathematical formula in Claim 1 is fatal to Rackspace's attempt to apply the holdings of *Benson* and *Flook*. In *Benson*, the Supreme Court found that the claimed method recited a specific mathematical formula, that this formula was only useful in a digital computer, and that if patentability of the claim at issue was upheld, it would "wholly pre-empt the mathematical formula and in practical effect would be a patent on the algorithm itself." *Benson*, 409 U.S. at 72. The specific formula is discussed by the Supreme Court on pp. 66-67 of the opinion.

In *Flook*, the Supreme Court rejected a claim under 35 U.S.C. § 101 because it also recited a specific mathematical formula (and contained no other point of novelty). *Parker v. Flook*, 437 U.S. 584, 588 (1978). Claim 1 from *Flook* is reproduced below:

1. A method for updating the value of at least one alarm limit . . . comprising the catalytic chemical conversion of hydrocarbons wherein said alarm limit has a current value of B_0+K wherein B_0 is the current alarm base and K is a predetermined alarm offset which comprises:

(1) Determining the present value of said process variable, said present value being defined as PVL;

(2) Determining a new alarm base B_1 , using the following equation:
 $B_1=B_0(1.0-F)+PVL(F)$, where F is a predetermined number greater than zero and less than 1.0;

(3) Determining an updated alarm limit which is defined as B_1+GK ; and thereafter

(4) Adjusting said alarm limit to said updated alarm limit value.

Id. at 596-597. As can be seen in the preamble of the claim and in steps 1-3, a series of variables are defined (e.g., B_0+K and PVL), then the variables are used to determine a new base alarm value in step 2 (value B_1). Finally, an updated alarm value is calculated by adding B_1+GK . After reviewing this series of steps, the Supreme Court concluded that the "mathematical formula" was what one thinks of in terms of formula - it takes a series of definite inputs, applies

certain arithmetic operations to them, then generates a definite output. *Id.* at 586 (“Using the formula, an operator can calculate an updated alarm limit once he knows the original alarm base, the appropriate margin of safety, the time interval that should elapse between each updating, the current temperature (or other process variable), and the appropriate weighting factor to be used to average the original alarm base and the current temperature.”).

Thus, in both *Benson* and *Flook*, the Supreme Court prohibited the naked patenting of a particular mathematical formula, stating that such formulas were akin to “laws of nature” and free for anyone to use. *Id.* at 589. In *Flook*, the Court hedged its wording to some extent by signaling that mathematical equations could be part of a valid claim if it contained significant pre or post processing. *Id.* at 591 (“While a scientific truth, or the mathematical expression of it, is not patentable invention, a novel and useful structure created with the aid of knowledge of scientific truth may be.” (quoting *Mackay Radio & Tel. Co. v. Radio Corp. of America*, 306 U.S. 86, 94 (1939))).

These holdings, therefore, are not applicable to Claim 1 because it does not purport to cover any particular mathematical formula or algorithm and certainly does not explicitly recite one. Unlike the claims at issue in *Benson* and *Flook*, one cannot extract an equation from Claim 1 such as $E=mc^2$, $\text{Area} = \text{length} * \text{width}$, $PV=nRT$, or the algorithms expressly recited in the claims at issue in *Benson* and *Flook*. Given the lack of a mathematical equation, Claim 1 does not fall into the exception of being a “law of nature.”

B. Claim 1 is not an Abstract Expression

For an otherwise qualifying claim to be an “abstract expression”, the Federal Circuit has stated that the “disqualifying [abstract] characteristic should exhibit itself so manifestly as to override the broad statutory categories of eligible subject matter and the statutory context that

directs primary attention on the patentability criteria of the rest of the Patent Act.” *Research Corp. Techs. v. Microsoft Corp.*, 627 F.3d 859, 868 (Fed. Cir. 2010). The Federal Circuit went on to state that “this court notes that inventions with specific applications or improvements to technologies in the marketplace are not likely to be so abstract that they override the statutory language and framework of the Patent Act.” *Id.*

And that is the precise case at hand. The ‘697 Patent specifically describes certain aspects of the IEEE 754 Standard and discusses (and claims) perceived improvements to that Standard. See ‘697 Patent, Col. 4:32-48 (quoted above). Also as mentioned above, the processes and algorithms described in this Standard have been implemented in billions of microprocessors. Given the wide adoption of IEEE 754 and its incorporation to actual products in the marketplace, it cannot be said that the Standard itself is some abstract expression.

The improvement to this Standard recited by Claim 1 is likewise not abstract and is exactly the type of invention the Federal Circuit was referring to when it said “specific applications or improvements to technologies in the marketplace [*i.e.*, IEEE 754 Standard] are not likely to be so abstract that they override the statutory language and framework of the Patent Act.” In the ‘697 Patent, the specification explicitly discusses rounding an operand before a mathematical operation is performed on it, states that this is “contrary to the IEEE 754 rounding of results” (‘697 Patent, Col. 4:40-1) and then goes on to specifically claim such improvement. Thus, the “rounding before operating” improvement to the computing arts recited in Claim 1 is a definite and substantive advancement to a concrete industry standard. It should therefore not be lightly mischaracterized as some form of useless “abstract expression.”

In addition to the sequence of rounding an operand followed by an arithmetic operation, the “conversion” steps in Claim 1 (steps 1 & 4) also contribute to the efficiency by which certain

processors can process floating-point numbers. See '697 Patent, Col. 2:36-46. These steps require converting a floating-point number that is composed of three specific fields (a sign, exponent and mantissa) from one format to another before and after rounding the operand and performing an arithmetic operation. Uniloc asserts that, when analyzed in the context of the '697 Patent, these steps are also definite and not abstract.

Thus, when viewed in its entirety, Claim 1 recites a specific and definite improvement to a widely recognized international standard for processing floating-point numbers. These types of improvements have been explicitly recognized by the Federal Circuit as being "not likely" to be so abstract as to run afoul of 35 U.S.C. § 101, contrary to the arguments set forth by Rackspace.

C. Machine or Transformation Test is Not Dispositive

As has been realized by several Courts, "Information Age" inventions are less suited for analysis under the so-called Machine or Transformation (MoT) Test than traditional "Industrial Age" inventions. See *Prompt Med. Sys., L.P. v. AllscriptsMysis Healthcare Solutions, Inc.*, No., 6:10-CV-71, 2012 U.S. Dist. LEXIS 30694, at *12-13 (E.D. Tex. Feb. 13, 2012) ("The Federal Circuit and a plurality of the Supreme Court have recognized that the machine-or-transformation test, though particularly useful for evaluating the patentability of Industrial Age technology, may be less appropriate for evaluating technologies rooted in the Information Age.") (citing *Ultramercial, LLC v. Hulu, LLC*, 657 F.3d 1323, 1327 (Fed. Cir. 2011) ("While machine-or-transformation logic served well as a tool to evaluate the subject matter of Industrial Age processes, that test has far less application to the inventions of the Information Age.")). This realization coupled with the Supreme Court's *Bilski* decision has greatly lessened the importance of the MoT Test today. Accordingly, no analysis of Claim 1 under the MoT Test is presented herein. Instead, the analysis above proceeds as described in *Research Corp.* and in *Prompt Med.*

Sys., where, instead of determining whether the claim under scrutiny passes a particular test, the focus is on whether a claim that would otherwise be proper under 35 U.S.C. § 101 falls within one of the three recognized exceptions to patentability (laws of nature, physical phenomena, and abstract ideas).

VI. CLAIMS 2-28

Given Uniloc's representation that it will only be asserting Claim 1 in this lawsuit, Uniloc has not focused on the other claims in the '697 Patent - claims 2-28. Uniloc notes, however, these other claims have additional limitations that bear on an analysis under 35 U.S.C. § 101, despite arguments to the contrary from Rackspace in its Motion.

For example, Rackspace states that the "'697 Patent does not - and could not - assert that the . . . 'circuit(s)' referenced in [Claim 2] . . . represent 'new machinery'." Contrary to Rackspace's claim, the '697 Patent does exactly that. Claim 2 requires a "load primary control logic circuit." Claim 2 requires that this circuit operate in a mode for "load[ing] an exact number, load[ing] with implied maximal accuracy encoding, load[ing] with accuracy encoding only for normal numbers and not for underflow or overflow numbers, and load[ing] with accuracy for all numbers." Several of these operations are identified with various objects of the invention. See '697 Patent, Col. 4:57 - 5:13. Given the close tie between the language of Claim 2 and the various objects of the invention, Rackspace's sweeping comment that this language adds nothing to the § 101 analysis is simply wrong. Instead, Claim 2 adds meaningful restrictions to Claim 1 by including the use of hardware that performs operations central to the inventive aspects of the '697 Patent.

Another example - independent Claim 22 has five elements written in means-plus-function language that would require an analysis under 35 U.S.C. § 112, ¶ 6 to properly analyze

its structural elements. Rackspace has attempted no such undertaking. Instead, Rackspace makes misleading statements such as “Claim 22, for example, recites ‘means for performing an arithmetic operation.’ . . . The patent nowhere claims that [this] hardware element [is] anything more than [a] standard [element] of a general purpose computer.” Rackspace Motion, p. 13. The full element being cited to by Rackspace is a “means for performing an arithmetic operation upon at least one converted floating-point value based upon said selected accuracy and rounding.” The ‘697 Patent contrasts the arithmetic unit of the present invention with a unit operating according to the IEEE Standard:

Once rounded, floating-point addition, subtraction, multiplication and division is performed in the arithmetic circuit logic block 62 using the two modified operands. It should be understood that for the present invention, the arithmetic computations are performed on pairs of operands representing a range of values, whereas the IEEE 754 floating-point operands represent single binary numbers.

‘697 Patent, Col. 12:17-23 (emphasis added). In light of this disclosure that specifically differentiates the operation of the arithmetic circuit logic block (referred to in Claim 22 as the “means for performing an arithmetic operation”) from the operation of a prior art arithmetic logic unit, Rackspace’s claim that the “means for performing an arithmetic operation” is a “standard element of a general purpose computer” should be dismissed.

Rackspace’s goes on to make other generalized arguments with respect to the other elements in Claim 22, as well as the other claims of the ‘697 Patent. These arguments suffer from similar deficiencies as the ones noted above. Rackspace picks and chooses various claim elements to focus on and mischaracterizes various portions of the specification, but never presents a full analysis of any particular claim. Given this lack of scrutiny, Rackspace certainly has not met its burden of proving that *each and every* claim of the ‘697 Patent is invalid under 35 U.S.C. § 101 by clear and convincing evidence. But, given Uniloc’s statement that it is willing

to stand or fall on Claim 1, a claim by claim analysis, by either party, is not believed to be necessary for disposition of Rackspace's Motion.

VII. CONCLUSION

For the foregoing reasons, Claim 1 of the '697 Patent does not fall within any of the Supreme Court's narrow, specific exceptions to patentability under 35 U.S.C. § 101. Therefore, Rackspace's "request[] that the Court dismiss [Uniloc's] Complaint" under Rule 12(b)(6) should be denied. Rackspace Motion, p. 17.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on the 13th day of September, 2012, I electronically filed the foregoing document with the clerk of the court for the U.S. District Court, Eastern District of Texas, Tyler Division, using the electronic case filing system of the court. The electronic case filing system sent a “Notice of Electronic Filing” to the attorneys of record who have consented in writing to accept this Notice as service of this document by electronic means.

/s/ Barry J. Bumgardner